L Number	Hits	Search Text	DB	Time stamp
1	115	(air with gap) and ((dielectric or insulating or insulative or insulator) with (opening or hole or via or trench or recess or aperture)) and (etch near3 stop) and @ad<20011005	USPAT; US-PGPUB	2004/06/12 09:10
4	5	(air with gap) and ((dielectric or insulating or insulative or insulator) with (opening or hole or via or trench or recess or aperture)) and (etch near3 stop)	EPO; JPO; DERWENT; IBM_TDB	2004/06/12 09:09
5	18	(air with void) and ((dielectric or insulating or insulative or insulator) with (opening or hole or via or trench or recess or aperture)) and (etch near3 stop) and @ad<20011005	USPAT; US-PGPUB	2004/06/12 09:10

L Number	Hits	Search Text	DB	Time stamp
1	1	("6350672").PN.	USPAT; US-PGPUB	2004/06/12 09:47
2	2	(("6057224") or ("5880018")).PN.	USPAT; US-PGPUB	2004/06/12 09:48
3	22	(air with gap) and ((opening or hole or recess or aperture or trench or via) with (dielectric or insulating or insulator or insulative)) and (etching adj stop)	USPAT; US-PGPUB	2004/06/12 10:53
4	17	((air with gap) and ((opening or hole or recess or aperture or trench or via) with (dielectric or insulating or insulator or insulative)) and (etching adj stop)) and @ad<20011005	USPAT; US-PGPUB	2004/06/12 10:53
5	4	(air with gap) and ((opening or hole or recess or aperture or trench or via) with (dielectric or insulating or insulator or insulative)) and (etching adj stop)	EPO; JPO; DERWENT; IBM_TDB	2004/06/12 10:34
6	157	((opening or hole or recess or aperture or trench or via) with (dielectric or insulating or insulator or insulative)) and (etching adj stop) and pecvd	USPAT; US-PGPUB	2004/06/12 10:53
7	97	(((opening or hole or recess or aperture or trench or via) with (dielectric or insulating or insulator or insulative)) and (etching adj stop) and pecvd) and @ad<20011005	USPAT; US-PGPUB	2004/06/12 11:15
8	37	PICVD and @ad<20011005	USPAT; US-PGPUB	2004/06/12 11:18
9	7	(PICVD with PECVD) and @ad<20011005	USPAT; US-PGPUB	2004/06/12 11:17
10	37	PICVD and @ad<20011005	USPAT; US-PGPUB	2004/06/12 11:18

US-PAT-NO: 6277732

DOCUMENT-IDENTIFIER: US 6277732 B1

TITLE: Method of planarizing inter-metal dielectric layer

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Application Filing Date - AD (1):
19990618

Brief Summary Text - BSTX (13):
To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a process for planarizing an inter-metal dielectric layer. A substrate having a plurality of metal lines thereon is provided. Some metal lines are formed close to each other, resulting in densely packed metal line regions. In contrast, some of the metal lines are laid further apart, resulting in loosely packed metal line regions. A dielectric liner layer is formed covering the metal lines and the exposed substrate. A nitridation treatment of the dielectric liner layer is carried out. Organic dielectric layer having a low dielectric constant is deposited over the dielectric liner layer so that the densely packed metal line regions are completely filled while the loosely packed metal line region is only partially filled. Using the dielectric liner layer as an **etching stop** layer, the organic dielectric layer is etched by performing a reactive ion etching operation. Inorganic dielectric layer having a low dielectric constant is deposited over the organic dielectric layer. The

inorganic dielectric layer has a thickness greater than the height of the metal lines. A cap dielectric layer is formed over the inorganic dielectric layer, and the cap dielectric layer is planarized by performing a chemical-mechanical polishing operation. A **via** is formed through the cap **dielectric** layer, the inorganic **dielectric** layer, the organic **dielectric** layer and the **dielectric** liner layer such that a top surface of the metal line is exposed. An electron beam curing operation is carried out so that the organic **dielectric** layer on the sidewall of the **via** is more dense. Lastly, a barrier layer and a metal plug are sequentially formed inside the via.

Detailed Description Text - DETX (5):

A dielectric liner layer 206 is formed over the metal lines 202a, 202b, 202c and the top surface of the substrate 200. The dielectric liner layer 206, for example, can be a silicon oxide layer formed using tetra-ethyl-ortho-silicate (TEOS) and oxygen as gaseous reactants in a plasma enhanced chemical vapor deposition (**PECVD**) process. If the percentage of oxygen within the gaseous reactant is dropped when the dielectric liner layer 206 is formed, a thicker liner layer 206a is formed on the top surface of the metal lines 202a, 202b and 202c while a thinner liner layer 206b is formed on the sidewalls of the metal lines 202a, 202b and 202c. A thicker liner layer on the top surface of the metal lines 202a, 202b and 202c can prevent some damages of the metal lines caused by subsequent etch operations. Meanwhile, a thinner liner layer on the sidewalls of metal lines 202a, 202b and 202c can lower the overall dielectric constant of the inter-metal dielectric layer between two adjacent metal lines. This is because although dielectric liner layer generally has a higher

dielectric constant, decreasing thickness of the sidewall liner layer 206b
leaves more room for the deposition of more low k dielectric material. Hence,
the overall dielectric constant is actually reduced.

Detailed Description Text - DETX (9):
To ensure that all the gaps in the densely packed metal line regions such as
204a are completely filled while the loosely packed metal line regions such as
204b are only partially filled, a reactive ion etching (RIE) operation of the
organic dielectric layer 208 may be additionally carried out using the
dielectric liner layer 206 as an **etching stop** layer. FIG. 1C shows the
external profiles of the respective organic dielectric layers 208a and 208b
within the densely packed metal line regions 204a and the loosely packed metal
line regions 204b after the RIE operation.

Detailed Description Text - DETX (13):
As shown in FIG. 1E, photolithographic and etching techniques are used to
form a **via** 214 that passes through the cap **dielectric** layer 212, the inorganic
dielectric layer 210, the organic **dielectric** layer 208 and the **dielectric** liner
layer 206. The via 214 exposes a portion of the metal line 202b. An electron
beam curing process is carried out so that the exposed sidewalls of the organic
dielectric layer 208 inside the **via** 214 are densed. If a RIE step is performed
after the organic dielectric layer 208 is formed, the electron beam curing
process can be omitted.

Claims Text - CLTX (6):
performing a reactive ion etching operation on the organic dielectric layer
using the dielectric liner layer as an **etching stop** layer;